REMARKS

In an Office Action mailed on January 21, 2005, claims 8-14, 21-26, 29, 30, 34-36 and 40-42 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite; and claims 8-14, 21-26, 29, 30, 34-36 and 40-42 were rejected under 35 U.S.C. § 102(e) as being anticipated by Taruishi.

Although Applicant disagrees with the basis for the § 112 rejections, for purposes of expediting prosecution, the claims have been amended to remove the language at the basis of the § 112 rejections. Therefore, for at least this reason, withdrawal of the § 112 rejections is requested.

The § 102 rejections are addressed below.

Rejections of Claims 8-12:

The method of independent claim 8 has been amended to recite that in response to a read operation occurring over a memory bus, data signal that are received directly from the memory bus into a memory controller are amplified. Furthermore, as amended, independent claim 8 recites disabling the amplification at the conclusion of the read operation.

Contrary to the limitations of amended independent claim 8, Taruishi only describes one set of amplifiers that amplify data signals that are received directly from a memory bus, i.e., amplifiers that are associated with the data input circuit 3. Thus, as previously pointed by the Applicant, these amplifiers are discussed in connection with lines 6-38 in column 11 of Taruishi. The other sense amplifiers described in Taruishi, such as, for example, the sense amplifiers discussed in lines 59-67 in column 5 through lines 1-40 in column 6 of Taruishi are amplifiers that amplify signals provided by the complimentary bit lines of the memory. Thus, referring to the only amplifier disclosed in Taruishi that is associated with a memory bus operation, it is clear in Taruishi that these amplifiers are activated in response to a write command, i.e., the command initiated in response to a write operation. This is logical in that in a memory device, such as the memory device that is disclosed in Taruishi, data signals are amplified from the memory bus only in a memory write operation, not a read operation.

Thus, although, as acknowledged by the Examiner, Taruishi describes a read operation occurring over a memory bus, there is no teaching or suggestion of the amplification of data signals from a memory bus in Taruishi's memory device, in that such an operation would be inconsistent with a memory device. Furthermore, although the Examiner states that the phrase "memory controller" may be "broadly considered" Applicant reminds Examiner that the construction must be reasonable. Thus, one skilled in the art recognizes that the phrase "memory controller" has a specific meaning and does not include merely any device that is associated with a memory.

Thus, for at least the reasons that are set forth above, amended independent claim 8 overcomes the § 102 rejection in view of Taruishi. Claims 9-12 are patentable for at least the reason that these claims depend from an allowable independent claim.

Rejections of Claims 21-23:

The memory controller of independent claim 21 has been amended to recite amplifiers that, in response to a read operation occurring over a memory bus, amplify data signals that are received directly from the memory bus.

See discussion of independent claim 8 above. In particular, Taruishi neither teaches nor even suggests the amplification of data signals that are received directly from a memory bus, as specifically set forth in independent claim 21. Thus, the sense amplifiers referred to the Examiner in Taruishi are sense amplifiers that amplify complimentary bit lines of the semiconductor memory device. The differential amplifier of the input buffer 3 amplifies signals from a memory bus. However, the amplification occurs in connection with a write operation, not a read operation.

Therefore, for at least any of the reasons that are set forth above, amended independent claim 21 overcomes the § 102 rejection in view of Taruishi.

Claims 22 and 23 are patentable for at least the reason that these claims depend from an allowable independent claim.

Rejections of Claims 29 and 30:

As amended, the computer system of independent claim 29 includes a memory and a memory controller. The memory controller includes amplifiers.

See discussion of independent claims 8 and 21 above. For at least the reason that Taruishi fails to teach or suggest the amplifiers that are recited in claim 29, withdrawal of the § 102(e) rejections of claims 29 and 30 is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102 and 112 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0668US).

Respectfully submitted,

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